Blog - MEMS New Product Development, Critical Design and Process Steps for Successful Prototypes (Part 2), David DiPaola, DiPaola Consulting, LLC, www.dceams.com

The fourth article of the MEMS new product development blog is Part 2 of the critical design and process steps that lead to successful prototypes. In the last article, the discussion focused on definition of the customer specification, product research, a solid model and engineering analysis to validate the design direction. The continuation of this article reviews tolerance stacks, DFMEA, manufacturing assessment and process mapping.

A tolerance stack is the process of evaluating potential interferences based on the interaction of components' tolerances. On a basic level, a cylinder may not fit in a round hole under all circumstances if the cylinder's outside diameter is on the high size and the inside diameter of the hole is on the lower size causing an interference when there is an overlap of their tolerances. This situation can become complex when multiple components are involved because it results in the number of variables reaching double digits. A simple approach to tolerance stacks is using a purely linear or worst case approach where full tolerances are added to determine potential for interference. However, experience from producing millions of sensors shows this approach is overly conservative and a non optimal design practice. If tolerances of the assembly follow a normal distribution, are statistically independent, are bilateral and are small relative to the dimension, a more realistic approach is a modified root sum of the squares (MRSS) tolerance stack technique. In this approach the root sum of the squares of the tolerances are multiplied by a safety factor to determine the maximum or minimum geometry for a set of interrelated components. The safety factor accounts for cases where RSS assumptions are not fully true. This approach is only recommended when 4 or more tolerances are at play. If only 2 tolerances are present as in the first example above, it is recommended to perform a linear tolerance stack. In some cases, linear tolerances need to be added to a MRSS calculation (MRSS calculation + linear tolerances = result). Pin position inside a clearance slot for anti-rotation is linear tolerance that is added to a MRSS calculation. Reasoning for this is the pin can be any location in the slot at any given time and does not follow a normal statistical distribution.

An example of a MRSS tolerance stack is provided below to review this concept in more detail. Let's determine if the wirebond coming off of the sense element will interfere with the metal housing. A modified RSS tolerance stack shows line to line contact and only a small adjustment in the design is needed to resolve the issue. The linear tolerance stack shows a significant interference what requires a larger adjustment. Dimensions and tolerances are illustrative only.



<u>Figure 1</u> MEMS Sensor Package (mm)

Figure 2 Modified Root Sum Square Versus Linear Tolerance Stack Approaches

 $\begin{array}{l} 0.17 > \mathsf{SF}^*(((\mathsf{T1}^2) + (\mathsf{T2}^2) + (\mathsf{T3}^2) + (\mathsf{T4}^2) + (\mathsf{T5}^2))^{(}(0.5)) \Longleftrightarrow \mathsf{MRSS} \ \mathsf{Approach} \\ 0.17 > 1.2^*((0.01^2 + 0.05^2 + 0.025^2 + 0.10^2 + 0.08^2)^{(}0.5)) = 0.17 \\ 0.17 > \mathsf{T1} + \mathsf{T2} + \mathsf{T3} + \mathsf{T4} + \mathsf{T5} \leftrightsquigarrow \mathsf{Linear} \ \mathsf{Approach} \\ 0.17 > 0.01 + 0.05 + 0.025 + 0.1 + 0.08 = 0.27 \end{array}$

An excellent text on this subject is *Dimensioning and Tolerancing Handbook*, by Paul J. Drake, Jr. and published by McGraw-Hill.

DFMEA, design failure mode and effects analysis. is another tool that is extremely effective to identify troublesome areas of the design that need to be addressed to prevent failures in validation and the field. Simply put this is a systematic approach to identify potential failure modes and their effects and finding solutions to mitigate the risk of a potential failure. A Risk Priority Number (RPN) is then established based on rating and multiplying severity, occurrence and detection of the failure mode (severity*occurrence*detection = RPN). The input to the tool is the design feature's function, the reverse of the design function, the effect of the desired function not being achieved, and the cause of the desired function not being achieved. There is also an opportunity to add design controls prevention and detection. The outputs are the corrective actions taken to mitigate risk of a potential failure. Figure 3 shows an brief example of this approach for a MEMS microphone.

Figure 3	
Design Failure Mode and Effects Analysi	is

Item / Process Function	Potential Failure Mode	Potential Effect(s) of Failure	S e v	Potential Cause(s)/ Mechanism(s) of Failure	O c u r	Current Design Controls Prevention	Current Design Controls Detection	D e t c	R. P. N.
Design Feature's Function	Reverse of the Desired Function	What is the Effect of the Desired Function Not being Achieved		What Caused the Desired Function Not to be Achieved					
Diaphragm of the capacitor deflects proportoinally with sound pressure	Diaphragm does not deflect at all	Microphone does not sense sound	9	Hole in diaphragm	2	Function test of microphone over sound range		1	18
	Diaphragm does not deflect proportionally with sound pressure	Microphone does not sense sound correctly	9	Crack in diaphragm	2	Function test of microphone over sound range		3	54
	Diaphragm does not deflect proportionally with sound pressure over temperature	Microphone does not sense sound correctly over temperature	Ø	lce formed on diaphragm	ß	Function test of microphone over sound range, temperature and humidity and after low temperature endurance validation		4	108

Further information on DFMEA can be found at Six Sigma Academy or AIAG. Corrective action section left out of illustration for clarity.

It is also extremely important that the manufacturing process be considered from the first day of the design process. Complete overlap of design and process development are the true embodiment of concurrent design. The following illustration depicts this well:



Hence before a MEMS design is started, discussions should be initiated with the foundry, component fabrication suppliers and the process engineers responsible for the package assembly. These meetings are excellent times to review new capabilities, initial ideas and explore new concepts. Considering the design from a process perspective simultaneously with other design requirements leads to highly manufacturable products that are often lowest cost. In essence, the design engineer is performing a constant manufacturing assessment with each step in the design phase. This methodology also encourages process short loops in the design phase to develop new manufacturing steps. This expedites the prototype process with upfront learning and provides feedback to the design team for necessary changes. The additional benefit of this approach is the boarder team is on board when prototyping begins as they had a say in shaping the design.

Another tool to thoroughly understand the process in the design phase is process mapping. Using this methodology, process inputs, outputs, flow, steps, variables, boundaries, relationships and decision points are identified and documented. The level of detail is adjustable and to start there can be a broad overview with more detailed added as the design progresses. This quickly provides a pictorial view of the process complexity, the variables effecting the design function, gaps, unintended relationships and non value added steps. It can also be used as a starting point for setting up the sample line in a logical order to assemble prototypes, estimating cycle time and establishing rework loops. To further clarify this method, a partial process map for a deep reactive ion etch process is provided:

Mask Type / Pattern Chemicals WEC - Offset / Type **Process Times** Chemical Photoresist Exposure Type Temperature Vacuum Levels Type and Vacuum Level / Time Quantity Bath Size Process Times Lamp Intensity / Time Time Flow Rate Process Temps Thickness Alignment Accuracy Temperature Agitation Canister RPM Wavelength Vacuum / None Drying RPM Pressure Cycle Profile Inputs Align Mask SOI Wafer RCA HMDS Spin Coat Cure and Photoresist Photoresist Clean Prime Expose Photoresist No Yes Hard Bake DRIE Measure Hole Reaches Develop Hole Depth Photoresist Photoresist Oxide Etch Loop Stop? **Chemical Mixture** Temperature Cleanliness Length and Depth And Quantity Atmosphere Power Of Measurement Rinse Time (Coil / Platen) Tip Speed Decision Agitation Vacuum Level Tip Size Temperature Time Gas Mixture And Flow Rate Cycle Times # of Loops

This process map is not all inclusive but illustrative of the process flow, critical parameters, inputs and a decision point. The personal protection equipment, tools used and relationships in the process are omitted for brevity. With this level of process detail available to the design team, the complexity of feature fabrication can be evaluated, anticipated variation from process parameters can be analyzed and much more possibly prompting design changes.

Knowledge of and attention to detail in these eight critical, yet often overlooked steps are essential in the design of highly manufacturable, low cost and robust products. These methodologies create a strong foundation upon which additional skills are built to provide a balanced design approach. In next month's blog, the design review process and a checklist will be discussed to help engineers prepare for this important peer review process.

Updated Bio:



David DiPaola is Managing Director for DiPaola Consulting a company focused on engineering and management solutions for electromechanical systems, sensors and MEMS products. A 17 year veteran of the field, he has brought many products from concept to production in high volume with outstanding quality. His work in design and process development spans multiple industries including automotive, medical, industrial and consumer electronics. He employs a problem solving based approach working side by side with customers

from startups to multi-billion dollar companies. David also serves as Senior Technical Staff to The Richard Desich SMART Commercialization Center for Microsystems, is an authorized external researcher at The Center for Nanoscale Science and Technology at NIST and is a Senior Member of IEEE. Previously he has held engineering management and technical staff

Figure 5 Partial Process Map of Deep Reactive Ion Etch Process

positions at Texas Instruments and Sensata Technologies, authored numerous technical papers, is a respected lecturer and holds 5 patents. To learn more, please visit www.dceams.com.